



Serial No. 09/396,228

RCA 89141 US

IN THE CLAIMS

1. (Original) In a remodulator system, apparatus for controlling the bit rate of an output packet stream, comprising:

a source of an input transport packet stream;

an input packet buffer, coupled to the input transport packet stream source, for generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;

an output packet stream generator, coupled to the input packet stream buffer, and responsive to an output clock signal, for generating the output packet stream in synchronism with the output clock signal,

a variable output clock signal generator, responsive to a control signal; and

a control signal generator, responsive to the status signal, and generating the control signal.

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FEB 27 2004

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2. (Original) The system of claim 1 wherein:

the variable output clock signal generator is responsive to the control signal for varying the frequency of the output clock signal; and

the control signal generator comprises circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is full, and decrease its frequency if the status signal indicates that the input packet buffer is empty.

3. (Original) The system of claim 2 wherein:

the input packet buffer generates the status signal further indicating whether the input packet buffer is: nearly full, or nearly empty;

the control signal generator further comprises circuitry to generate the control signal to condition the variable output clock signal generator to increase its frequency if the status signal indicates that the input packet buffer is nearly full, and decrease its frequency if the status signal indicates that the input packet buffer is nearly empty.

4. (Original) The system of claim 1 wherein:  
the input transport packet stream contains null packets; and  
if the status signal indicates that the input packet buffer is full, null packets are deleted from the input transport packet buffer.

5. (Original) The system of claim 1 further comprising:  
a source of additional packets; wherein:  
the output packet stream generator comprises a multiplexer, coupled to the input transport packet stream source and the additional packet source, for combining packets from the input transport packet stream and additional packets to generate the output packet stream.

6. (Original) The system of claim 5 wherein if the status signal indicates that the input packet buffer is empty, an additional packet is inserted into the output packet stream.

7. (Original) The system of claim 5 wherein the source of additional packets comprises:  
a source of packets representing auxiliary data; and  
a source of null packets; and  
the multiplexer inserts an auxiliary data packet into the output packet stream as an additional packet if an auxiliary data packet is available, and inserts a null packet into the output packet stream as an additional packet if an auxiliary data packet is not available.

8. (Original) In a remodulator system, a method for controlling the bit rate of an output packet stream, comprising the steps of:  
providing a source of an input transport packet stream;  
storing input packet from said source in an input packet buffer;  
generating a status signal indicating whether the input packet buffer is: full, empty, or neither empty nor full;  
generating the output packet stream in synchronism with the output clock signal;

generating a variable output clock signal in response to a control signal; and  
generating the control signal in response to the status signal.

9. (Original) The method of claim 8 wherein:  
the frequency of the output clock signal varies in response to the control signal, and  
the variable output clock signal increases in frequency if the status signal  
indicates that the input packet buffer is full, and decreases in frequency if the status  
signal indicates that the input packet buffer is empty.

10. (Original) The method of claim 9 wherein:  
the status signal further indicates whether the input packet buffer is: nearly full,  
or nearly empty; and  
the control signal conditions the variable output clock signal to increase its frequency  
if the status signal indicates that the input packet buffer is nearly full, and decrease its  
frequency if the status signal indicates that the input packet buffer is nearly empty.

11. (Original) The method of claim 8, wherein:  
the input packet stream format is compatible with one of a QAM or QPSK  
modulation format; and  
the output packet stream format is compatible with an 8-VSB or 16-VSB  
modulation format.

12. (Original) The method of claim 8, wherein:  
the source of input transport packet stream represents auxiliary on-screen display  
(OSD) information.

13. (Original) The method of claim 8, wherein:  
the input packet stream format is compatible with one of QAM, QPSK or VSB  
modulation formats; and  
the output packet stream format is compatible with a different one of said QAM,  
QPSK or VSB modulation formats.